MAGNETIC BUBBLE MEMORY
INTERFACE APPLICATION NOTES

COIL DRIVER CIRCUIT

The objective of the coil drive arrangement is to develop between 48 and 54 Oersteds peak field strength in the bubble memory using a triangular current waveform. The technique used to implement this is to apply a step voltage across the inductors (coils) until the peak current is developed. The voltage is then removed which allows the current to reverse through diode paths provided by the diode array. Ideally, the upward slope should equal the downward slope to provide a symmetrical triangular waveform. However, in the case of the BK10103/BCA0101 evaluation board the downward slope is greater than the upward slope due to the fact that different voltages are produced during the two time periods under consideration. In addition, the diodes begin to go out of conduction when the current approaches zero during the collapse period. This gives rise to possibility of oscillation until the drive cycle is applied. To correct for these factors, a small amount of drive period overlap is applied which means the drive period is lengthened and the collapse period is shortened. Lead lengths should be kept reasonably short to reduce noise and high frequency oscillations. Ceramic decoupling capacitors must be located close to the coil drivers and diode arrays.

Several factors combine to determine the overall peak in-plane magnetic field that determines bubble propagation via the permalloy T-bars. These factors fall into three catagories: mechanical, voltage, and time. Since a step voltage drive scheme is used, the inductance of the coil directly affects the slope of the current waveform. Slight variations in wire diameter or deformations that affect the volume of the coil will affect the coil inductance. The voltage across the coil terminals can be affected by power supply tolerance and variations in drive transistors and diodes as a function of temperature and current amplitude. The amount of time the drive pulse is applied is determined by the accuracy of the frequency source. To prevent cumulative tolerance build-up, the frequency tolerance is specified to be quite accurate as this is the easiest parameter to control. The next easiest area to control is power supply tolerance-with mechanical tolerances being most difficult to maintain.

FUNCTION DRIVER CIRCUIT

The transfer, generate, and replicate elements operate in the current mode rather than the voltage mode. The resistances of these elements vary considerably from device to device. This dictates that constant current sources/sinks be used to maintain the accurate range of current required for optimum operation. Futhermore, the current to the replicate and generate elements must be reduced as the temperature is increased since bubbles are produced easier at high temperatures. An overdrive condition in the generate section can result in multiple bubble generation while an overdrive condition in the replicate area can mean generation of bubbles as opposed to duplication. Actually the generator can be overdriven as a function of time as typical generation time is less than 100 nesc.

The constant current sources on the BK10103/BKA0103 evaluation board do not have temperature compensation. The currents can be changed by varying the +12v supply input to each current source to compensate for temperature. For normal room temperature evaluation these inputs have been designed to be connected to +12v. The logic inputs to the constant current sources should be stable before drive voltage (+12v) is applied to prevent transients upon power up/down.

SENSE AMPLIFIER CIRCUIT

The raw unattenuated signal from the detector of the bubble memory is typically 15 mv peak. Unfortunately this signal contains a large amount of high frequency noise and a significant offset voltage. The raw signal is processed through a simple passive network which results in a clean signal but with a reduced amplitude of typically 3 mv peak. The sense amp is implemented with an internal AC restore circuit. The clamp signal determines the reference voltage so that the data may be sampled a short time later after the signal has reached its peak amplitude. To reduce the effects of noise, the timing of the clamp and strobe signals is fairly critical. The dual detectors are used in a bridge network to allow some degree of common mode noise reduction. For optimum operation the current in each detector should be matched as accurately as possible. The best operating current is 5.5 ma in each detector. Current magnitudes in excess of 8 ma can cause permanent damage to the detector elements. The detector load resistors (R17, R18) on the BK10103/BKA0103 evaluation boards have been specified as ± 5% tolerance, but should actually be ± 1%. The desired sensing threshold is between 0.8 and 1.2 mv. In some cases the MC1444 sense amp that is being used temporarily has a threshold less than 0.8 mv. These sense amplifiers will have to be hand selected for the time being to give the best error rates. The sense amp being developed at TI will have a controlled threshold of 1.0 ± 0.2 mv. Short signal lead lengths are imperative. Avoid placing noise generating signal or power supply leads in the area of the detection leads. The sense amp or its passive attenuation network should not be placed next to the exposed (lead) end of the bubble memory.

INTERFACE SIGNALS

Board enable (BDEN, P1-E) allows the use of several bubble memory evaluation boards with a common controller. For single bubble memory systems, this signal can be grounded (logic zero).

The other mnemonics are defined as follows:

CXA	- X COIL DRIVE POS.	XIN	- TRANSFER-IN ENABLE
CXB	- X COIL DRIVE NEG.	XOUT	- TRANSFER-OUT ENABLE
CYA	- Y COIL DRIVE POS.	REP	- REPLICATE ENABLE
CYB	- Y COIL DRIVE NEG.	ANN	- ANNIHILATE ENABLE
CLAMP	- AC RESTORE	GEN	- GENERATE ENABLE
STROBE	- DETECTOR STROBE	DAT	- DATA FROM BUBBLE

The +17v supply is being used temporarily to provide base drive to the 75325 output drive circuit and also serves as a source for the detector load resistors. This power supply will be eliminated with the introduction of the custom interface integrated circuits.

POWER SUPPLY SEQUENCE

To prevent the possibility of burning out the generate and/or replicate elements in the bubble memory IC, it is necessary to have the controlling logic in a stable condition before applying drive voltage.

For the BK10103/BKA0103 evaluation board, the +12 volt supply should be the last supply to be turned on and the first supply to be turned off. The sequence of the other supplies should not matter.

Also the TTL input lines that control the generate and replicate elements must be stable before the +12 volt supply is applied. For this reason, it is suggested that the logic supply for the bubble memory evaluation board be common with the control logic.

POWER SUPPLY ACCURACY

The +12v supply directly determines the current amplitude for the transfer, replicate, and generate elements. The relative accuracy required for the control elements is listed below in rank order - most accurate listed first:

1. TRANSFER OUT
2. TRANSFER IN
3. REPLICATE
4. GENERATE

Therefore, for optimum operation, the +12v supply should be adjusted to give the most accurate transfer out current. The other currents should then be checked for operation within specified limits.

The +12v supply also determines coil current. Many of the bubble memories manufactured to date may require that the +12v supply be increased as much as a volt to give the value of coil current listed in the specification. This may mean that there be two independently adjustable +12v supplies for the evaluation board to accommodate the exacting requirements of the coils and control elements both. This conflicting situation will be rectified in the near future.

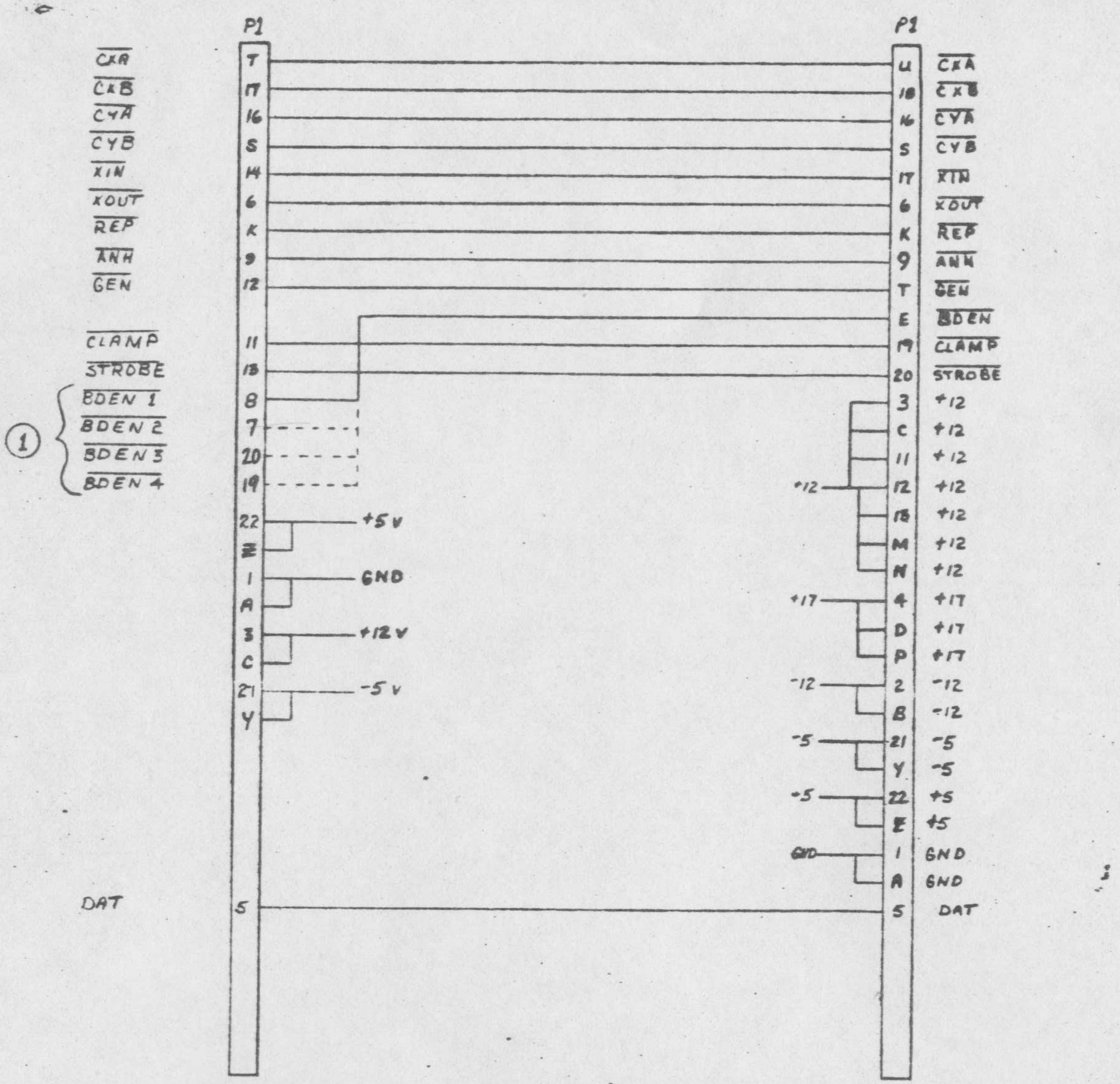
Pin 2 and B of the BK10103/BKA0103 evaluation board have previously been shown connecting to -5v. This connection should be changed to -12v. Several of the devices shipped to date have transfer resistances that exceed the values shown in the specification. Possible stauration of the output stage of the current source could occur giving marginal operation. Changing from -5v to -12v corrects this situation.

The other power supplies should be adjusted for a ± 5% operating range as measured at the evaluation board connector. Ripple and noise should be held within normal limits for proper TTL operation.

EVALUATION PROCEDURE

Since the bubble memory is vulnerable to incorrect timing pulses and/or amplitudes, it is best to check all the aforementioned before plugging the bubble into its location on the board.

Timing signals can be checked at the connector without the circuit card being connected. With an untested BK10103, resistors can be substituted for the bubble memory. Typical resistances of the various elements are listed in the specification. Current loops are provided on the evaluation card to allow checking of coil and control element currents with an oscilloscope current probe. Detector current can be calculated by measuring the voltage across the detection load resistors (R17, R18). Once it has been determined that everything is operational, the bubble memory may then be inserted into position. With the bubble memory in place, extreme care should be exercised when probing the card to prevent accidental shorting of signals which could burn out a control element.



CONTROLLER CARD
BC10103/BCA0103

MAGNETIC BUBBLE
MEMORY EVALUATION
CARD - BK10103/BKA0103

(1) FOUR BOARD ENABLE ($\overline{\text{BDEN}}$) CONNECTIONS ARE PROVIDED TO ALLOW USE OF UP TO FOUR BUBBLE EVALUATION CARDS FROM A SINGLE CONTROLLER CARD. IN THIS CONFIGURATION ONE OF FOUR BUBBLE CARDS IS SELECTED AT A GIVEN TIME TO OPERATE WITH THE CONTROLLER CARD.

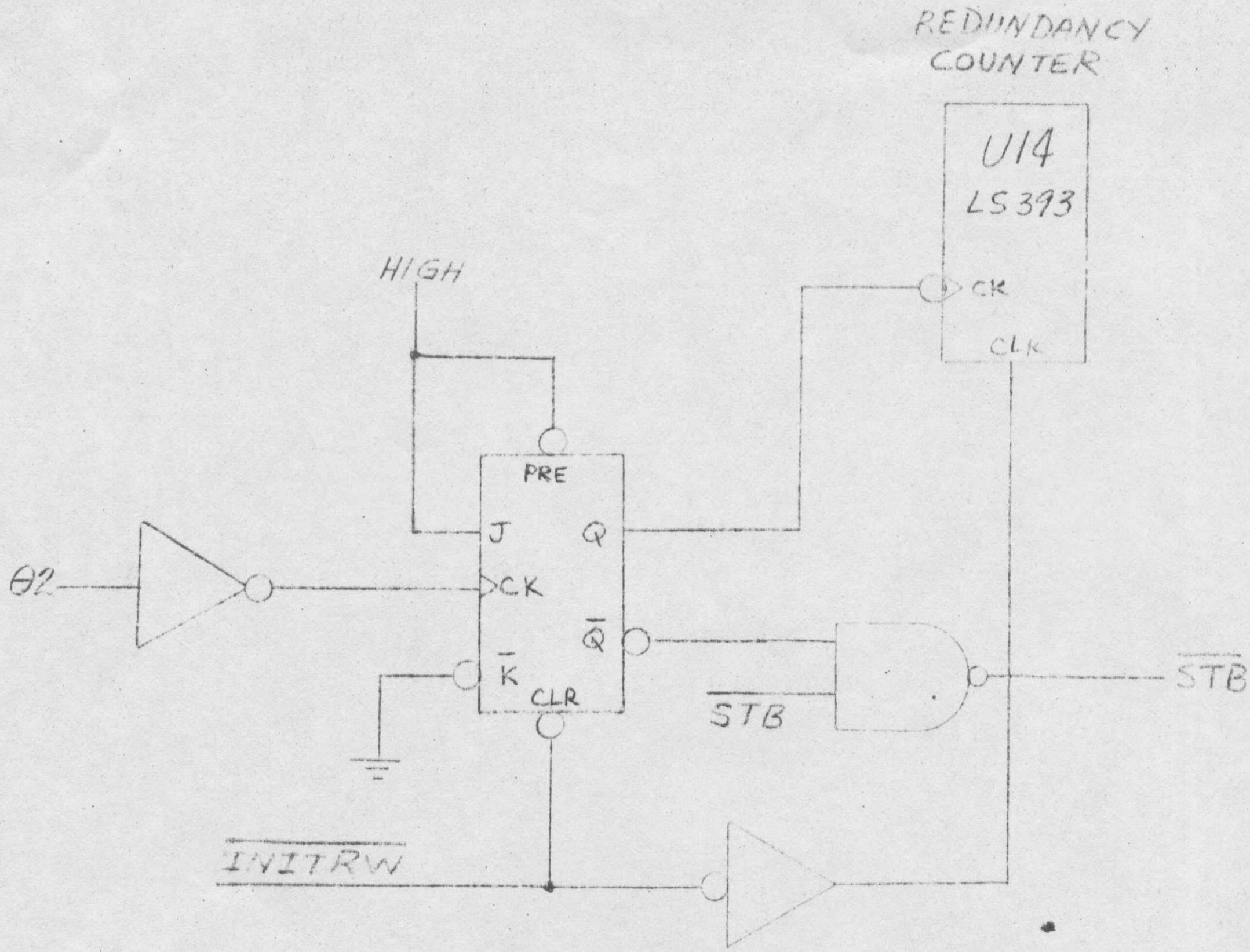
MATERIAL:	
PROCESS:	
NEXT ASSEMBLY	
TOLERANCES UNLESS SPECIFIED	
DRAFTSMAN / DATE	.XXX ± .010 .XX ± .020 .X ± .030
ENGR / DATE: CS 1-20-78	
CHECKED / DATE	
ENGINEER / DATE	
APPROVED / DATE: EMC 1-21-78	MATERIAL
RELEASED / DATE	BOUGHT

TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR OPERATIONS

CODE IDENT NO 01295

TITLE: WIRING DIAGRAM, INTER-CONNECT BETWEEN MBM EVALUATION AND CONTROL CARDS

SIZE C | SHEET 1/1



THIS CIRCUIT GENERATES A 50KHz CLOCK TO REPLACE GC50 TO ALLOW OPERATION WHEN THE LOOP CLOSEST TO THE DETECTOR IS DECLARED DEFECTIVE. THE MULTI-PAGE MODE DOES NOT OPERATE PROPERLY AT THE TIME OF THIS WRITING. A SOLUTION IS EXPECTED IN THE NEAR TERM. THE PRINTED CIRCUIT BOARD DOES NOT REQUIRE ANY MODIFICATION IN THE SINGLE-PAGE MODE IF THE FIRST LOOP IN THE BUBBLE MEMORY IS DECLARED GOOD.

January 26, 1978

IMPORTANT NOTICE

Great care should be employed to assure that the generate and replicate elements do not receive pulse widths or amplitudes greater than specified. The result of an overstress will be a fused element.

Writing into bad loops is not an option. Some bad loops will have defects that may reproduce bubbles from normal coil field drives. The reproduced bubbles may eventially contaminate the entire chip. There are procedures to clear the memory if this happens, but only as a last resort.

The proms included in this kit are not programmed. Programming service is available through most TI Supply Companies. It is recommended that sockets be installed on the printed circuit board for the proms and the TMS9916.

The 74S471 (U10) prom provides the function timing information and its map is included. Locations not listed should not be programmed. The letter X indicates optional programming.

The redundancy prom (U11) can provide up to four bubble maps. For single bubble systems, it is suggested that prom section D01 (pin 12) be programmed. To select output D01, connector P2-pins 4,18, and 16-should be grounded.

Proms U1 and U2 are used to set up an effective address for the bubble memory subsystem. The following logic equations apply for the outputs of U1:

$$\overline{CS} = (\text{Valid subsystem address}) \bullet \overline{(MEMEN)}$$

$$\overline{READ} = (\text{Valid subsystem address}) \bullet \overline{(MEMEN)} \bullet (DBIN)$$

$$WRITE = (\text{Valid subsystem address}) \bullet \overline{(MEMEN)} \bullet \overline{(DBIN)}$$

The output of U2 should be as follows:

$$D01 = (\text{Valid subsystem address})$$

SPECIFICATION CHANGES

EFFECTIVE JULY 1, 1977

TIMING TABLE

Replicate	LE	5.35	± .156
	Dur	1.57	± .156
Annihilate	LE	3.6	± .156
	Dur	4.7	± .156
Generate	LE	.46	± .156
	Dur	.23	± .156
X-Out	LE	1.3	± .156
	Dur	1.87	± .156
X-In	LE	5.16	± .156
	Dur	2.4	± .156

AMPLITUDE EQUATIONS

Replicate	135 - 0.57T
Annihilate	60
Generate	280 - 1.2 T
X-Out	44 - 0.09 T
X-In	30

COIL DRIVE REQUIREMENTS

Additional requirements on coil drive.

1. Dead zone -the time commutation to zero current and the start of the next linear ramp must be less than 50 nanseconds.

2. Assymetry - the ratio of the time between a zero cross and the next peak to the time between the same peak and the next zero crossing must be between 1 and 1.5.

3. Noise - high frequency deviations from a linear ramp must be less than 5mA in amplitude.

4. Non-linearity - low frequency deviations from a linear ramp due to source impedance of the driver and other sources must be less than 8% of the amplitude of an ideal linear ramp at all times.

5. DC current in the drive coils must not exceed 10mA at any time.

6. Turnoff ring -any ringing when either drive field is turned off must not exceed 10mA positive or negative.